## Microcontroller (EEC421)

## Lecture 8

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## Microcontroller

## Lecture 8: ARITHMETIC OPERATIONS

$\checkmark$ Introduction
$\checkmark$ Flags
$\checkmark$ Instructions Affecting Flags
$\checkmark$ Incrementing and Decrementing
$\checkmark$ Addition :Unsigned and Signed Addition
$\checkmark$ Multiple-Byte Signed Arithmetic
$\checkmark$ Subtraction :Unsigned and Signed Subtraction
$\checkmark$ Multiplication and Division
$\checkmark$ Decimal Arithmetic
$\checkmark$ Applications of microcontrollers often involve performing mathematical calculations on data in order to alter program flow and modify program actions. The domain of the microcontroller is that of controlling events as they change (real-time control).
$\checkmark$ A sufficient number of mathematical opcodes must be provided, however, so that calculations associated with the control of simple processes can be done, in real time, as the controlled system operates. When faced with a control problem, the programmer must know whether the 8051 has sufficient capability to expeditiously handle the required data manipulation. If it does not, a higher performance model must be chosen.

- The arithmetic opcodes are grouped into the following types:


## Mnemonic

INC destination
DEC destination
$\mathrm{ADD} / \mathrm{ADDC}$ destination, source
SUBB destination, source MUL AB

DIV AB
DA A

## Operation

Increment destination by 1
Decrement destination by I
Add source to destination without/with carry (C) flag
Subtract, with carry, source from destination
Multiply the contents of registers A and B
Divide the contents of register A by the contents of register B
Decimal Adjust the A register

- A key part of performing arithmetic operations is the ability to store certain results of those operations that affect the way in which the program operates.
- For example, adding together two one-byte numbers results in a one-byte partial sum, because the 8051 is an eight-bit machine. But it is possible to get a 9-bit result when adding two 8-bit numbers.
- The ninth bit must be stored also, so the need for a one-bit register, or carry flag in this case, is identified. The program will then have to deal with the ninth bit, perhaps by adding it to a higher order byte in a multiple-byte addition scheme. Similar actions may have to be taken when a larger byte is subtracted from a smaller one. In this case, a borrow is necessary and must be dealt with by the program.
- Not all instructions change the flags, but many a programming error has been made by a forgetful programmer who overlooked an instruction that does change a flag.
- The 8051 has four arithmetic flags: the carry (C), auxiliary carry (AC), overflow (OV), and parity (P).
$\checkmark \quad$ The C. AC, and OV flags are arithmetic flags. They are set to 1 or cleared to 0 automatically, depending upon the outcomes of the following instructions.
$\checkmark \quad$ The following instruction set includes all instructions that modify the flags and is not confined to arithmetic instructions:

| INSTRUCTION MNEMONIC | FLAGS AFFECTED |  | remember that the flags are all stored in the PSW. |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ADD | $C$$C$ | $\begin{aligned} & \text { OV } \\ & \text { ov } \end{aligned}$ |  |  |  |  |  |  |  |  |
| ADDC |  |  |  |  |  |  |  |  |  |  |
| ANL C, drect | $c$ |  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CINE | ${ }_{C}^{C}=0$ |  | Cr | ${ }_{\text {AC }}$ | F0 | RS1 | RSO | ov | - | p |
| CLPC $C P L C$ | $\begin{aligned} & C=\frac{0}{C} \\ & C= \end{aligned}$ |  | Cr | AC | F0 | RS1 | RSO | ov | - | P |
| DAA | C |  |  |  |  |  |  |  |  |  |
| DIV | $c=0$ | OV |  |  |  |  |  |  |  |  |
| MOV C, direct | $c$ |  |  |  |  |  |  |  |  |  |
| MuL | $\mathrm{C}=0$ | OV |  |  |  |  |  |  |  |  |
| ORL C.direct | c |  |  |  |  |  |  |  |  |  |
| RLC | c |  |  |  |  |  |  |  |  |  |
| RRC | C |  |  |  |  |  |  |  |  |  |
| SETB C | $\mathrm{C}=1$ |  |  |  |  |  |  |  |  |  |
| sube | C AC | OV |  |  |  |  |  |  |  |  |

$\checkmark$ A flag may be used for more than one type of result. For example, the C flag indicates a carry out of the lower byte position during addition and indicates a borrow during subtraction.
$\checkmark$ The parity flag is affected by every instruction executed. The $P$ flag will be set to a 1 if the number of 1 's in the $A$ register is odd and will be set to 0 if the number of 1 's is even.

## Incrementing and Decrementing

* The simplest arithmetic operations involve adding or subtracting a binary 1 and a number.
* These simple operations become very powerful when coupled with the ability to repeat the
* Operation that is, to "INCrement" or "DECrement" -until a desired result is reached.
* Register, Direct, and Indirect addresses may be INCremented or DECremented.
* No math flags (C, AC, OV) are affected.


## Mnemonic

INC A
INC Rr
INC add
INC@Rp
INC DPTR
DEC A
DEC Rr
DEC add
DEC@Rp

## Operation

Add a one to the A register
Add a one to register Rr
Add a one to the direct address
Add a one to the contents of the address in Rp
Add a one to the 16 -bit DPTR
Subtract a one from register $A$
Subtract a one from register Rr
Subtract a one from the contents of the direct address
Subtract a one from the contents of the address in register Rp

* Example:

Mnemonic
MOV A, \#3Ah DEC A
MOV R0,\#15h
MOV 15h,\#12h
INC @R0
DEC 15 h
INC R0
MOV 16h,A INC @R0
MOV DPTR, \#12FFh
INC DPTR DEC 83h

Operation
$A=3 A h$
$A=39 h$
$R 0=15 h$
Internal RAM address $15 \mathrm{~h}=12 \mathrm{~h}$
Internal RAM address $15 \mathrm{~h}=13 \mathrm{~h}$
Internal RAM address $15 \mathrm{~h}=12 \mathrm{~h}$
$\mathbf{R 0}=16 \mathrm{~h}$
Internal RAM address $16 \mathrm{~h}=39 \mathrm{~h}$
Internal RAM address $16 \mathrm{~h}=3 \mathrm{Ah}$
DPTR $=12 \mathrm{FFh}$
DPTR $=1300 \mathrm{~h}$
DPTR $=1200 \mathrm{~h}(\mathrm{SFR} 83 \mathrm{~h}$ is the DPH byte)

- All addition is done with the A register as the destination of the result.
- All addressing modes may be used for the source: an immediate number, a register, a direct address, and an indirect address.
- Some instructions include the carry flag as an additional source of a single bit that is included in the operation at the least significant bit position.


## Mnemonic

ADD A.\#n
ADD A, Rr
ADD A,add
ADD A.@Rp

## Operation

Add A and the immediate number $n$; put the sum in A
Add A and register Rr ; put the sum in A
Add A and the address contents; put the sum in A
Add A and the contents of the address in Rp; put the sum in A

Note that the $C$ flag is set to 1 if there is a carry out of bit position 7 ; it is cleared to 0 otherwise. The AC flag is set to 1 if there is a carry out of bit position 3 ; it is cleared otherwise. The OV flag is set to 1 if there is a carry out of bit position 7 , but not bit position 6 or if there is a carry out of bit position 6 but not bit position 7, which may be expressed as the logical operation

$$
\mathrm{OV}=\mathrm{C} 7 \mathrm{XOR} \mathrm{C} 6
$$

## Unsigned and Signed Addition

- Signed numbers use bit 7 as a sign bit in the most significant byte (MSB) of the group of bytes chosen by the programmer to represent the largest number to be needed by the program.
- Bits 0 to 6 of the MSB, and any other bytes, express the magnitude of the number. Signed numbers use a 1 in bit position 7 of the MSB as a negative sign and a 0 as a positive sign. Further, all negative numbers are not in true form, but are in 2's complement form.
- In signed form, a single byte number may range in size from $10000000 b$, which is -128 d to 01111111 b , which is +127 d . The number 00000000 b is OOOd and has a positive sign, so there are 128d negative numbers and 128d positive numbers.


## Unsigned and Signed Addition

## - Unsigned Addition

$\checkmark$ Unsigned numbers make use of the carry flag to detect when the result of an ADD operation is a number larger than FFh. If the carry is set to one after an ADD, then the carry can be added to a higher order byte so that the sum is not lost. For instance,

$$
\begin{aligned}
95 \mathrm{~d} & =01011111 \mathrm{~b} \\
\frac{189 \mathrm{~d}}{284 \mathrm{~d}} & =\frac{10111101 \mathrm{~b}}{100011100 \mathrm{~b}}=284 \mathrm{~d}
\end{aligned}
$$

The $C$ flag is set to 1 to account for the carry out from the sum. The program could add the carry flag to another byte that forms the second byte of a larger number.

## Unsigned and Signed Addition

- Signed Addition
$\checkmark$ If unlike signed numbers are added, then it is not possible for the result to be larger than -l28d or +127 d , and the sign of the result will always be correct.
$\checkmark$ If positive numbers are added, there is the possibility that the sum will exceed + 127d, as demonstrated in the following example:
$-001 \mathrm{~d}=1111111 \mathrm{~b}$
$+027 \mathrm{~d}=\frac{00011011 \mathrm{~b}}{000011010 \mathrm{~b}}=+026 \mathrm{~d}$

$$
\begin{aligned}
& +045 \mathrm{~d}=00101101 \mathrm{~b} \\
& \frac{+075 \mathrm{~d}}{+120 \mathrm{~d}}=\frac{01001011 \mathrm{~b}}{01111000 \mathrm{~b}}=120 \mathrm{~d}
\end{aligned}
$$

$$
\begin{aligned}
& +100 \mathrm{~d}=01100100 \mathrm{~b} \checkmark \quad \text { oV flag } \\
& \frac{+050 \mathrm{~d}}{+150 \mathrm{~d}}=\frac{00110010 \mathrm{~b}}{10010110 \mathrm{~b}}=-106 \mathrm{~d}
\end{aligned}
$$

## Unsigned and Signed Addition

## - Signed Addition

$$
\begin{aligned}
& -070 \mathrm{~d}=10111010 \mathrm{~b} \\
& -070 \mathrm{~d}=\frac{10111010 \mathrm{~b}}{-140 \mathrm{~d}}=1110100 \mathrm{~b}=+116 \mathrm{~d}
\end{aligned}
$$

Or, the magnitude can be interpreted as -12 d , which is the remainder after a carry out of -128d. In this example, there is a carry from bit position 7, and no carry from bit position 6 , so the carry and the OV flags are set to 1 . The magnitude of the sum is correct; the sign bit must be changed to a 1 .

| FLAGS |  |
| :--- | :--- |
| $\mathbf{C}$ | $\mathbf{O V}$ |
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 1 | 1 |

## ACTION

None
Complement the sign None
Complement the sign
A general rule is that if the OV flag is set, then complement the sign. The OV flag also signals that the sum exceeds the largest positive or negative numbers thought to be needed in the program.

## Add with Carry Mnemonics:

ADDC A, \#n

ADDC A,add

ADDC A, Rr ADDC A,@Rp

Add the contents of A , the immediate number n , and the C flag; put the sum in A
Add the contents of A , the direct address contents, and the C flag; put the sum in $A$
Add the contents of A , register Rr , and the C flag; put the sum in A Add the contents of A , the contents of the indirect address in Rp, and the C flag; put the sum in A

- Subtraction can be done by taking the 2's complement of the number to be subtracted, the subtrahend, and adding it to another number, the minuend. The 8051, however, has commands to perform direct subtraction of two signed or unsigned numbers.
- Register A is the destination address for subtraction. All four addressing modes may be used for source addresses. The commands treat the carry flag as a borrow and always subtract the carry flag as part of the operation.

Mnemonic<br>SUBB A, \#n<br>SUBB A,add<br>SUBB A,Rr<br>SUBB A,@Rp

## Operation

Subtract immediate number $n$ and the $C$ flag from $A$; put the result in $A$
Subtract the contents of add and the C flag from A ; put the result in A Subtract Rr and the C flag from A ; put the result in A Subtract the contents of the address in Rp and the C flag from A ; put the result in A

## Subtraction

$$
\text { SUBB } \begin{aligned}
& 015 \mathrm{~d}=00001111 \mathrm{~b} \\
& \frac{100 \mathrm{~d}}{-085 \mathrm{~d}}=\frac{01100100 b}{10101011 \mathrm{~b}}=171 \mathrm{~d}
\end{aligned}
$$

The C flag is set to 1 , and the $O V$ flag is set to 0 . The 2 's complement of the result is 085 d . The reverse of the example yields the following result:

$$
\begin{aligned}
& 100 \mathrm{~d}=01100100 \mathrm{~b} \\
& \frac{015 \mathrm{~d}}{085 \mathrm{~d}}=\frac{00001111 \mathrm{~b}}{01010101 \mathrm{~b}}=085 \mathrm{~d}
\end{aligned}
$$

The C flag is set to 0 , and the OV flag is set to 0 . The magnitude of the result is in true form.

## Signed Subtraction

$$
\begin{aligned}
+100 \mathrm{~d} & =01100100 \mathrm{~b} \quad \text { (Carry flag }=0 \text { before SUBB }) \\
\text { SUBB }+126 \mathrm{~d} & =\frac{01111110 \mathrm{~b}}{-026 \mathrm{~d}}: 11100110 \mathrm{~b}=-026 \mathrm{~d}
\end{aligned}
$$

There is a borrow into bit positions 7 and 6 ; the carry flag is set to 1 , and the OV flag is cleared.

$$
\begin{aligned}
-061 \mathrm{~d} & =11000011 \mathrm{~b} \quad(\text { Carry flag }=0 \text { before SUBB }) \\
\text { SUBB } \frac{-116 \mathrm{~d}}{+055 \mathrm{~d}} & =\frac{10001100 \mathrm{~b}}{00110111 \mathrm{~b}}=+55 \mathrm{~d}
\end{aligned}
$$

There are no borrows into bit positions 6 or 7 , so the OV and carry flags are cleared to zero.

$$
\begin{aligned}
-099 d & =10011101 b \quad \text { (Carry flag }=0 \text { before SUBB }) \\
\text { SUBB }+100 d & =\frac{01100100 b}{-199 d} \quad 00111001 b
\end{aligned}=+057 d \quad .
$$

Here, there is a borrow into bit position 6 but not into bit position 7; the $O V$ flag is set to 1 , and the carry flag is cleared to 0 . Because the OV flag is set to 1 , the result must be adjusted. In this case, the magnitude can be interpreted as the 2 's complement of 71 d , the remainder after a carry out of 128 d from 199 d . The magnitude is correct, and the sign needs to be corrected to a 1 .

## Subtraction

## Example:

Mnemonic<br>MOV 0DOh, \#00h<br>MOV A, \#3Ah<br>MOV 45h, \#13h<br>SUBB A,45h<br>SUBB A,45h<br>SUBB A,\#80h<br>SUBB A.\#22h<br>SUBB A, \#0FFh

Operation
Carry flag $=0$
$\mathrm{A}=3 \mathrm{Ah}$
Address $45 \mathrm{~h}=13 \mathrm{~h}$
$\mathrm{A}=27 \mathrm{~h} ; \mathrm{C}=0, \mathrm{OV}=0$
$A=14 \mathrm{~h} ; \mathrm{C}=0, \mathrm{OV}=0$
$A=94 \mathrm{~h} ; \mathrm{C}=1, \mathrm{OV}=1$
$A=71 \mathrm{~h} ; \mathrm{C}=0, \mathrm{OV}=0$
$A=72 h ; C=1, O V=0$

- The 8051 has the capability to perform 8-bit integer multiplication and division using the $A$ and $B$ registers. Register $B$ is used solely for these operations and has no other use except as a location in the SFR space of RAM that could be used to hold data.
- The A register holds one byte of data before a multiply or divide operation, and one of the result bytes after a multiply or divide operation.
- Multiplication and division treat the numbers in registers $A$ and $B$ as unsigned. The programmer must devise ways to handle signed numbers.


## - Multiplication

## Mnemonic Operation

MUL $A B$
Multiply A by B; put the low-order byte of the product in A, put the high-order byte in B
The OV flag will be set if $\mathrm{A} \times \mathrm{B}>\mathrm{FFh}$. Setting the OV flag does not mean that an error has occurred. Rather, it signals that the number is larger than eight bits, and the programmer needs to inspect register B for the high-order byte of the multiplication operation. The carry flag is always cleared to 0 .

Mnemonic<br>MOV A.\#7Bh<br>MOV 0FOh. \#02h<br>MUL AB<br>MOV A, HOFEh<br>MUL AB

Operation
$\mathrm{A}=7 \mathrm{Bh}$
$B=02 h$
$A=00 \mathrm{~h}$ and $\mathrm{B}=\mathrm{F} 6 \mathrm{~h}$ : OV Flag $=0$
$A=F E h$
$A=14 \mathrm{~h}$ and $\mathrm{B}=\mathrm{F} 4 \mathrm{~h} ;$ OV Flag $=1$

## Multiplication and Division

## - Division

## Division

Division operations use registers A and B as both source and destination addresses for the operation. The unsigned number in register $\mathbf{A}$ is divided by the unsigned number in register B , as indicated in the following table:

| Mnemonic | Operation <br> DIV AB |
| :--- | :--- |
| Divide A by B; put the integer part of quotient in register $A$ and the <br> integer part of the remainder in B |  |

The OV flag is cleared to 0 unless B holds 00h before the DIV. Then the OV flag is set to I to show division by 0 . The contents of A and B , when division by 0 is attempted, are undefined. The carry flag is always reset.

| Mnemonic | Operation |
| :--- | :--- |
| MOV A,\#0FFh | $A=F F h(255 \mathrm{~d})$ |
| MOV OFOh, \#2Ch | $B=2 \mathrm{C}(44 \mathrm{~d})$ |
| DIV AB | $\mathrm{A}=05 \mathrm{~h}$ and $\mathrm{B}=23 \mathrm{~h}[255 \mathrm{~d}=(5 \times 44)+35]$ |
| DIV AB | $\mathrm{A}=00 \mathrm{~h}$ and $\mathrm{B}=05 \mathrm{~h}[05 \mathrm{~d}=(0 \times 35)+5]$ |
| DIV AB | $\mathrm{A}=00 \mathrm{~h}$ and $\mathrm{B}=00 \mathrm{~h}[00 \mathrm{~d}=(0 \times 5)+0]$ |
| DIV AB | $\mathrm{A}=?$ ? and $\mathrm{B}=? ?$ OV flag is set to one |

## Decimal Arithmetic

- Most 8051 applications involve adding intelligence to machines where the hexadecimal numbering system works naturally. There are instances, however, when the application involves interacting with humans, who insist on using the decimal number system. In such cases, it may be more convenient for the programmer to use the decimal number system to represent all numbers in the program.
- Four bits are required to represent the decimal numbers from 0 to 9 (0000 to 1001) and the numbers are often called Binary coded decimal (BCD) numbers. Two of these BCD numbers can then be packed into a single byte of data. The 8051 does all arithmetic operations in pure binary. When BCD numbers are being used the result will often be a non-BCD number, as shown in the following example


## Decimal Arithmetic

$$
\begin{aligned}
49 \mathrm{BCD} & =01001001 \mathrm{~b} \\
+38 \mathrm{BCD} & =\frac{00111000 \mathrm{~b}}{87 \mathrm{BCD}}
\end{aligned}
$$

Note that to adjust the answer, an 06d needs to be added to the result.

```
Mnemonic Operation
DA A Adjust the sum of two packed BCD numbers found in A register; leave
    the adjusted number in A.
```

- The C flag is set to I if the adjusted number exceeds 99BCD and set to 0 otherwise. It is important to remember that the DA A instruction assumes the added numbers were in BCD before the addition was done. Adding hexadecimal numbers and then using DA A will not convert the sum to BCD.
- The DA A opcode only works when used with ADD or ADDC opcodes and does not give correct adjustments for SUBB, MUL or DIV operations. The programmer might best consider the ADD or ADDC and DA A as a single instruction and use the pair automatically when doing BCD addition in the 8051.


## Decimal Arithmetic

Mnemonic
MOV A, \#42h
ADD A, \#13h DA A
ADD A, \#17h DA A
ADDC A,\#34h DA A
ADDC A,\#11h
DA A

Operation
$\mathrm{A}=42 \mathrm{BCD}$
$\mathrm{A}=55 \mathrm{~h} ; \mathrm{C}=0$
$A=55 ; C=0$
$A=6 \mathrm{Ch} ; \mathrm{C}=0$
$A=72 B C D ; C=0$
$A=A 6 h ; C=0$
$A=06 B C D ; C=1$
$A=18 B C D ; C=0$
$A=18 B C D ; C=0$

